POWER TRANSISTOR SAFE OPERATING AREA — SPECIAL CONSIDERATIONS FOR SWITCHING POWER SUPPLIES

INTRODUCTION

The power transistor, in today's switching power supply, exists in an environment which is quite hostile to semiconductors. Large currents, large voltages, high temperature, high frequency, and low impedance sources add up to something close to the worst of all possible worlds for the transistor.

Given this type of environment, it is not surprising to find that keeping transistor stresses within acceptable limits can be quite a challenge. Transistors designed and specified specifically for switching power supplies help, but do not in themselves guarantee a reliable design. Very often, reliability is determined by the more subtle aspects of how stress imposed by the power supply relates to transistor safe operating area.

The purpose here is to take a look at some of these subtleties, and differentiate those stresses that the transistor can handle from those it can not. In order to provide a proper foundation, special considerations are preceded with a review of forward bias and reverse bias safe operating area.

REVIEW OF FORWARD BIAS SAFE OPERATING AREA (FBSOA)

Forward bias safe operating area measures the ability of the transistor to handle stress when its base is forward biased. The FBSOA curve contains maximum limits for both steady state dissipation and turn-on load lines. Both aspects are examined.

Definition

Forward bias safe operating area is defined for conditions in which the base is forward biased. Since it is possible to have a positive base-emitter voltage and negative base current during storage time, forward bias is defined in terms of base current. The FBSOA curve applies when turn-on base current (I_{B1}) is flowing, or when the base is open circuited. When turn-off base current is flowing, even if the source is merely a resistor from base to emitter, reverse bias safe operating area applies.

The short pulse width FBSOA curve is the load line boundary for turn-on switching. The typical transistor data sheet shows a 5 to 10 microsecond curve. The shorter of the two makes a practical boundary for turn-on load lines.

To complete the definition, it is appropriate to specify a means of measurement. Forward bias safe operating area is measured in a common base test circuit. A simplified schematic is illustrated in Figure 1. This type of circuit allows reasonable precision in defining the three FBSOA variables: collector-emitter voltage, collector current, and time, without having to change input conditions for each transistor.

Voltage Sensitivity

Power transistors are a great deal more sensitive to voltage stress than they are to stress imposed by large collector currents. This is particularly true of bipolar transistors, and shows up readily on the FBSOA curve. Using the curve in Figure 2 as an example, it is easy to show just how significant this voltage sensitivity is.

At Point A, allowable power dissipation is 3.33 volts × 150 amps = 500 watts. As the thermal limit portion of the curve is traversed to Point B, there is no change in power dissipation, 50 amps × 10 volts = 500 watts. However, when a point on the second breakdown portion of the curve is chosen at Point C, allowable power dissipation is reduced dramatically to 30 watts.

By definition, the second breakdown portion of the FBSOA curve is that portion in which allowable power dissipation is decreasing with increased voltage. The physics behind this phenomenon is explained with the aid of Figure 3.

Current density is superimposed upon the cross section of an emitter finger for two values of collector-emitter voltage, $V_{CE} = 10$ volts, and $V_{CE} = 100$ volts. It is evident from the figure, that current density increases dramatically as voltage rises. As the current density increases, the area in which power dissipation occurs decreases. In other words, the effective size of the transistor becomes smaller and smaller as its collector-emitter voltage is raised.

Looking one step further, increasing current density with collector voltage can be explained by collector-base depletion. As collector voltage is increased, depletion into the metallurgical base increases. The electrical base width is thereby narrowed, causing an increase in the lateral resistance of the base under-
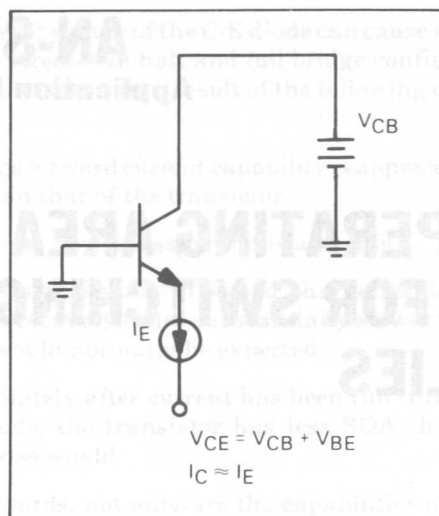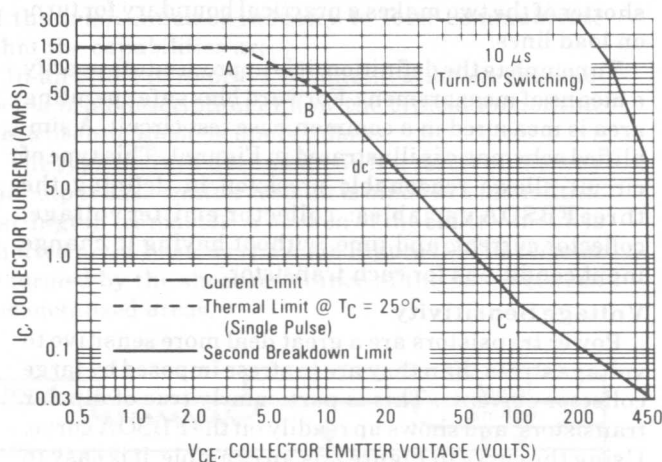
FIGURE 1 — FBSOA Test Circuit

$$V_{CE} = V_{CB} + V_{BE}$$
$$I_C \approx I_E$$

FIGURE 2 — FBSOA Curve (MJ10100)

Current Limit
Thermal Limit @ $T_C = 25°C$ (Single Pulse)
Second Breakdown Limit

neath the emitter. In turn, base current to the center of the emitter finger is choked off, limiting the amount of current flowing through the center of the finger. With very little current flowing through the center, current flow is restricted to the edges. This restriction results in a high current density at the edge, which gets higher as collector voltage is increased.

Before ending the discussion of voltage sensitivity, it is worth spending a few moments to consider $V_{CEO(sus)}$, the limit at the right hand side of the FBSOA curve. There is a point worthy of emphasis. Namely, that $V_{CEO(sus)}$ is an instantaneous limitation. Any excursion of the turn-on load line beyond $V_{CEO(sus)}$, or any condition where $V_{CE} > V_{CEO(sus)}$ with forward bias base current applied, risks failure of the transistor.

Temperature Derating

Temperature derating of FBSOA is a fairly straightforward procedure. However, keeping in mind the preceding discussion on voltage sensitivity, there is a right way and a wrong way to do it.

In the thermally limited region of the FBSOA curve, temperature derating is quite simple. Allowable power
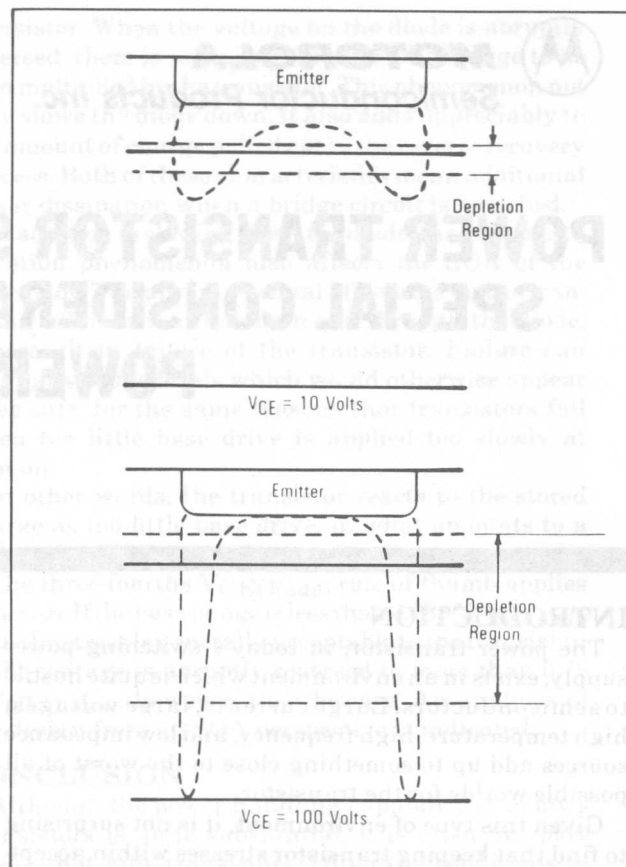

FIGURE 3 — Current Density Comparison

dissipation can be found at any case temperature according to the following equation:

$$P_D = (T_{J(max)} - T_C) R_{\theta JC}$$

Where: P_D = Maximum Allowable Power Dissipation
T_J = Junction Temperature
T_C = Case Temperature
$R_{\theta JC}$ = Junction to Case Thermal Resistance

If you prefer to use a curve, a derating factor may be obtained from Figure 4. This derating factor multiplied by the maximum power dissipation limit will yield the same result as the equation

It is in the second breakdown limited portion of the FBSOA curve that the right way, and the wrong way come into the picture. Due to the greater voltage sensitivity of the transistor, derating first starts with voltage and proceeds according to the following steps:

1. At any given voltage, determine maximum allowable power by reading current off the FBSOA curve and multiplying by the voltage.

2. Derate maximum allowable power at temperature, by applying the appropriate derating factor from the second breakdown derating curve in Figure 4.

3. Convert maximum allowable power into maximum allowable current by dividing the voltage into maximum allowable power.

4. Check to make sure that the thermal limit is not exceeded, it applies also.

This procedure is equally applicable to both the pulsed and dc forward bias SOA curves. It, therefore, applies to turn-on load lines as well as conditions of steady state power dissipation.
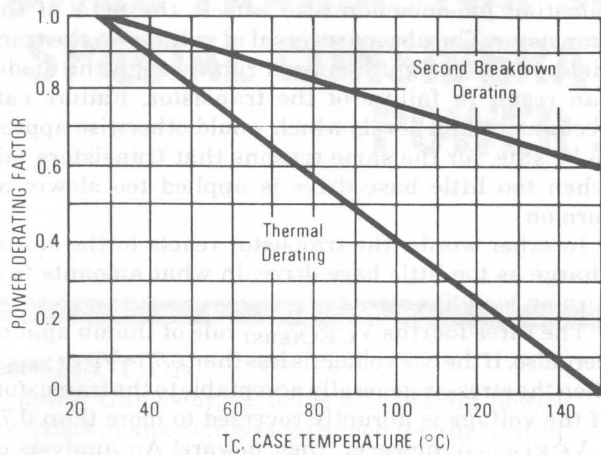

FIGURE 4 — Power Derating

REVERSE BIAS SAFE OPERATING AREA (RBSOA)

Reverse bias safe operating area is a measure of the transistor's ability to handle stress with its base reverse biased. The RBSOA curve represents the outer boundary for allowable turn-off load lines.

Definition

Reverse bias safe operating area is defined for conditions in which the base is reverse biased. Again, the definition is in terms of current. Reverse bias safe operating area applies to situations in which turn-off base current (I_{B2}) is flowing.

It is measured in the simple flyback circuit shown in Figure 5. The RBSOA curve is a measure of the simultaneous peak collector current and peak clamp voltage that the transistor can withstand in this circuit.

Forward and reverse bias safe operating area are analogous in many respects. One of these is voltage sensitivity. Bipolar power transistors exhibit the same sensitivity to voltage stress in the RBSOA mode that they do in forward bias conditions. It is easy to see from the RBSOA curve in Figure 6, that allowable peak instantaneous power decreases dramatically as voltage is increased.

There is a voltage limit beyond which the transistor will accept no stress. This limit is the collector-base breakdown voltage, commonly referred to in power transistor data sheets as V_{CEV}. Any excursion beyond V_{CEV} will cause device failure.

Temperature Derating

The analogy between forward and reverse bias safe operating area breaks down when it comes to temperature derating. Whereas forward bias SOA requires considerable derating with temperature, reverse bias

SOA is essentially independent of temperature. In fact, over the temperature range of 25°C to 100°C, RBSOA of the most commonly used switching power supply output transistors increases with increasing temperature.

This seemingly contradictory behavior is caused by a strong dependency of RBSOA upon collector resistivity. As temperature goes up, the effect of increasing collector resistivity with temperature predominates over the thermal effects. The result is RBSOA performance which is flat to slightly improving with temperature.
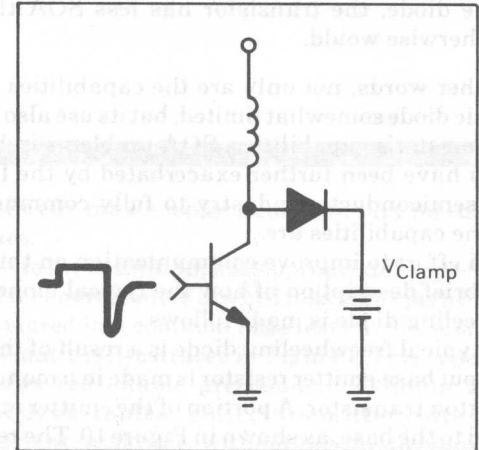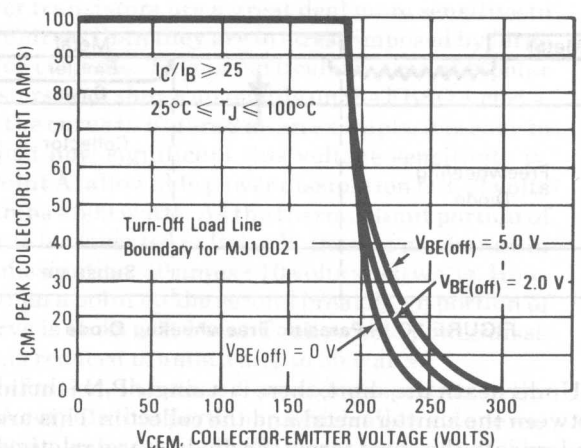

FIGURE 5 — RBSOA Test Circuit

FIGURE 6 — RBSOA Curve (MJ10021)

Time

The variables associated with an RBSOA curve are peak collector-emitter voltage (V_{CEM}), peak collector current (I_{CM}), and off-bias. Time does not appear in an RBSOA specification. It is an instantaneous limitation. The turn-off load line is not safe if it goes outside the RBSOA curve even for a brief instant. In fact it is the very short voltage spikes, associated with unclamped inductance, that are most likely to kill transistors at turn-off.

Obviously, in any SOA limit, time has to be factored in somehow. The off-bias variable in RBSOA specs indirectly establishes a time constraint. With a given

off-bias, the crossover time of the transistor will be limited to some maximum amount. This amount of time is built into the RBSOA curve.

Off-Bias

Off-bias has a very significant effect upon RBSOA performance. It has a large influence for the following two reasons:

1. Crossover time, and therefore, the amount of energy that the transistor sees, is heavily dependent upon off-bias.

2. Current crowding at turn-off is directly related to off-bias.

These concepts are illustrated in Figures 7 and 8.

From Figure 7, it is readily apparent that as off-bias is increased, the amount of energy in any given RBSOA condition decreases. This effect tends to improve RBSOA performance with increasing off-bias. On the other hand, Figure 8 shows how increasing off-bias increases current density during RBSOA stress. A lateral electric field associated with the off-bias increasingly constricts current flow to the center of the emitter finger, as off-bias is increased. This is very similar to the second breakdown effect in forward bias SOA, and tends to limit RBSOA performance.

With these two factors working against each other, it is possible to design power transistors such that RBSOA will either increase or decrease with increasing off-bias. The fact that manufacturers advertise RBSOA performance going in opposite directions, represents no real conflict. The divergent RBSOA performance merely reflects differences in transistor design.

SPECIAL CONSIDERATIONS FOR SWITCHING POWER SUPPLIES

Standard concepts of safe operating area provide the foundation that is needed for matching stress in the supply with transistor characteristics. However, there are subtleties peculiar to switching power supplies which are not directly addressed by the standard concepts. Some of the conditions which can lead to these subtleties are discussed here.

TURN-ON LOAD LINE

The importance of understanding subtle stresses starts right at the beginning, as the transistor is turning on. It is during turn-on that one of the common misconceptions about power transistor SOA comes into play. If asked to identify the most frequent cause of failure at turn-on, most designers would probably suspect a current voltage product which is too large for the transistor's capability.

Quite to the contrary, the short pulse SOA capability of the transistor is generally quite a bit larger than what most people would expect, and usually in considerable excess of what is specified on the data sheet. Most often it is not the combination of voltage and current stress that is at odds with the transistor's characteristics. It is usually the base drive that is causing an unacceptable level of stress.

From an SOA point of view, it is essential to provide the transistor with a generous amount of base drive VERY RAPIDLY at turn-on. It is usually the lack of
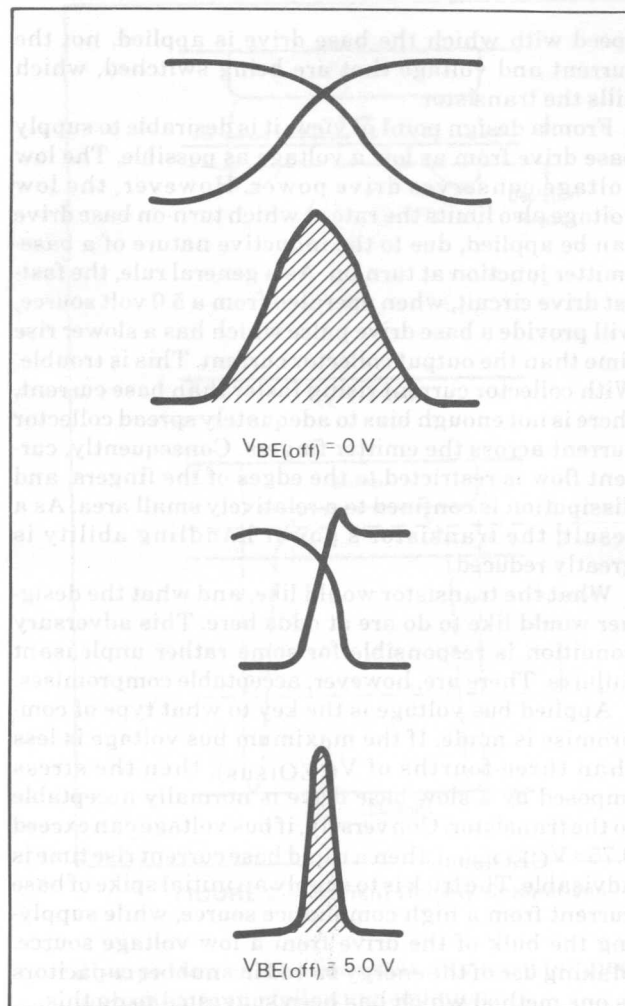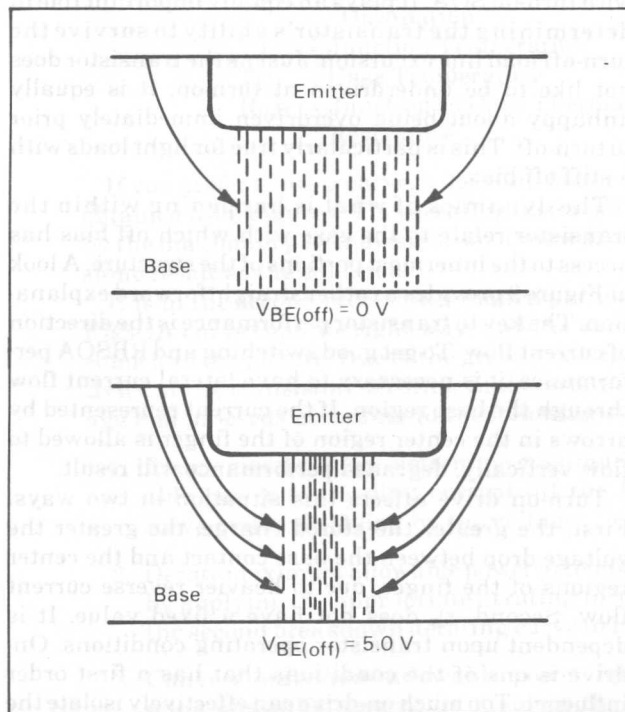

FIGURE 7 — RBSOA Energy Relationships

FIGURE 8 — RBSOA Current Crowding

speed with which the base drive is applied, not the current and voltage that are being switched, which kills the transistor.

From a design point of view, it is desirable to supply base drive from as low a voltage as possible. The low voltage conserves drive power. However, the low voltage also limits the rate at which turn-on base drive can be applied, due to the inductive nature of a base-emitter junction at turn-on. As a general rule, the fastest drive circuit, when operated from a 5.0 volt source, will provide a base drive pulse which has a slower rise time than the output collector current. This is trouble. With collector current rising faster than base current, there is not enough bias to adequately spread collector current across the emitter fingers. Consequently, current flow is restricted to the edges of the fingers, and dissipation is confined to a relatively small area. As a result, the transistor's power handling ability is greatly reduced.

What the transistor would like, and what the designer would like to do are at odds here. This adversary condition is responsible for some rather unpleasant failures. There are, however, acceptable compromises.

Applied bus voltage is the key to what type of compromise is made. If the maximum bus voltage is less than three-fourths of $V_{CEO(sus)}$, then the stress imposed by a slow base drive is normally acceptable to the transistor. Conversely, if bus voltage can exceed $0.75 \times V_{CEO(sus)}$, then a rapid base current rise time is advisable. The trick is to supply an initial spike of base current from a high compliance source, while supplying the bulk of the drive from a low voltage source. Making use of the energy stored in snubber capacitors is one method which has been suggested to do this.

TURN-OFF LOAD LINE

The importance of on-state base drive does not end with turn-on SOA. It plays an equally important role in determining the transistor's ability to survive the turn-off load line excursion. Just as the transistor does not like to be underdriven at turn-on, it is equally unhappy about being overdriven immediately prior to turn-off. This is particularly true for light loads with a stiff off bias.

The dynamics of what is happening within the transistor relate to the ease with which off bias has access to the innermost portions of the structure. A look at Figure 9 provides a rather straightforward explanation. The key to transistor performance is the direction of current flow. To get good switching and RBSOA performance, it is necessary to have lateral current flow through the base region. If the current represented by arrows in the center region of the finger is allowed to flow vertically, degraded performance will result.

Turn-on drive affects this situation in two ways. First, the greater the stored charge, the greater the voltage drop between the base contact and the center regions of the finger, due to heavier reverse current flow. Second, r_b does not have a fixed value. It is dependent upon transistor operating conditions. On-drive is one of the conditions that has a first order influence. Too much on-drive can effectively isolate the center regions of the finger from turn-off bias.

When this happens, the result is slower switching

time and decreased RBSOA. In particular, some transistors can become quite fragile when base drive approaches collector current, and the off bias is fairly stiff.
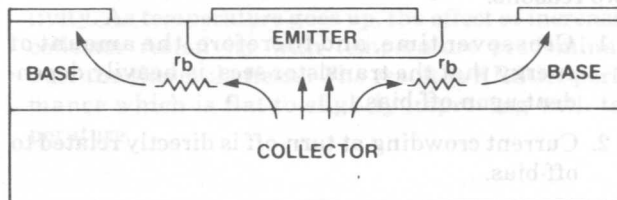

FIGURE 9 — Emitter Finger Crossection

If we look at turn-on drive from the designer's point of view, circuit design is simplified by having a fixed base drive. However, for a fixed base drive to work, enough current has to be supplied to satisfy the lowest gain transistor at maximum load and lowest temperature.

This type of drive scheme can easily result in the kind of situation which is illustrated as follows:

High Load . . . . I_{B1} = 2A, Ic(pk) = 10A

Low Load . . . . I_{B1} = 2A, Ic(pk) = 2A

Again, there is an adversary relationship between the designer's ideal preference, and the needs of the transistor. The later condition, in this example, is trouble. The capability of the transitor to withstand turn-off stress in the 2.0 amp/2.0 amp condition will, in all probability, be significantly less than if it were pulling the full 10 amp load current.

Fortunately, maximizing the transistor's performance is relatively straightforward, in many applications. Either proportional base drive or a baker clamp can be used to eliminate the gross overdrive that occurs with fixed base drive. From the transistor's point of view, the baker clamp is by far the preferred of these two techniques. By providing each individual transistor with as much base drive as it needs, and no more, both switching and reverse safe area are optimized.

POWER UP/POWER DOWN

Before leaving the subject of load lines, the conditions that can occur when the power supply is turned-on or turned-off merit a few words. When the supply is turned on or off, the first or last switching cycle can have a load line that varies dramatically from steady state operation. As Murphy's Law would have it, these one-cycle load line excursions have a tendancy to stress the transistor more severely than the steady state.

It pays to look closely at these first and last cycles. One cyle is all it takes to kill a perfectly healthy transistor. This is particularly true when the load line excursion exceeds safe voltage boundaries.

COLLECTOR-EMITTER DIODES

In the most popular high voltage darlington transistors, there is a diode between the collector and emitter terminals. Most often, this diode is a parasitic element.

The parasitic nature of the C-E diode can cause some subtle SOA stresses in half and full bridge configurations. These stresses are a result of the following characteristics:

1. Average forward current capability is appreciably less than that of the transistor.

2. Maximum power dissipation is also less.

3. Gain multiplication of stored charge results in reverse recovery times substantially slower than what would normally be expected.

4. Immediately after current has been run through the diode, the transistor has less SOA than it otherwise would.

In other words, not only are the capabilities of the parasitic diode somewhat limited, but its use also limits the transistor's capabilities. SOA problems in bridge circuits have been further exacerbated by the failure of the semiconductor industry to fully communicate what the capabilities are.

In an effort to improve communication on this subject, a brief description of how the typical monolithic freewheeling diode is made follows.

The typical freewheeling diode is a result of the way the output base-emitter resistor is made in a monolithic darlington transistor. A portion of the emitter metal is shorted to the base, as shown in Figure 10. The resistor is formed by the sheet resistance of the base between the metalized areas.
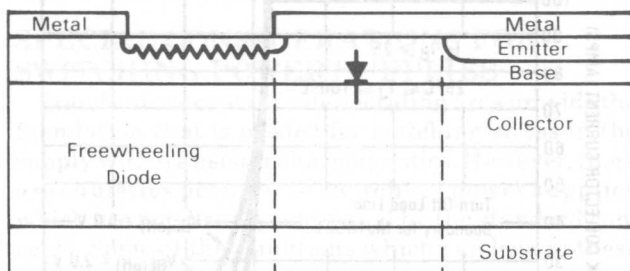

FIGURE 10 — Parasitic Freewheeling Diode

Underneath the short, there is a single P-N junction between the emitter metal and the collector. This area underneath the short forms the diode. It is a relatively small portion of the total collector-base junction. Consequently, it does not have the same power, or current handling capability as the transistor.

The parasitic nature of this diode also has some implications regarding its speed. During the time that forward current passes through the diode, charge is stored in its anode and cathode. Since the anode is the base of the transistor, and the cathode is the collector, charge is stored in the base-collector junction of the

transistor. When the voltage on the diode is abruptly reversed, there is an opportunity for this charge to be gain multiplied by the transistor. This phenomenon not only slows the diode down, it also adds appreciably to the amount of charge pulled out in the reverse recovery process. Both of these characteristics mean additional power dissipation when a bridge circuit is switched.

In addition to slowing down the diode, the gain multiplication phenomenon also affects the SOA of the transistor. The abrupt reversal of voltage on the transistor, after current has been run through the diode, can result in failure of the transistor. Failure can occur at voltage levels which would otherwise appear to be safe, for the same reasons that transistors fail when too little base drive is applied too slowly at turn-on.

In other words, the transistor reacts to the stored charge as too little base drive, in what amounts to a turn-on load line stress.

The three-fourths $V_{CEO(sus)}$ rule of thumb applies here also. If the bus voltage is less than $0.75 \times V_{CEO(sus)}$, then the stress is generally acceptable to the transistor. If the voltage is abruptly reversed to more than $0.75 \times V_{CEO(sus)}$, however, then beware! An analysis of the design from an SOA perspective is indicated.

CONCLUSION

Although the power handling capability of today's transistors is quite substantial, it is often not pure power that kills transistors. Often the conditions in which the transistor is asked to control the power are more important than the absolute amount. In these situations, there are many subleties. It is one area of power supply design where that fine line between science and art is crossed and recrossed.

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